

**What is claimed is:**

1           1.    A method of fabricating a nitride read only  
2 memory, comprising the steps of:  
3           providing a semiconductor substrate, comprising a  
4           memory region and a peripheral circuit region  
5           therein;  
6           growing a pad oxide on the semiconductor substrate;  
7           forming a plurality of parallel buried diffusion  
8           regions as bit lines in the memory region;  
9           forming a first shallow trench and a second shallow  
10          trench in the peripheral circuit region;  
11          conformally forming an ONO film on the semiconductor  
12          substrate;  
13          depositing a polysilicon layer on the ONO film to fill  
14          the first shallow trenches and the second shallow  
15          trench;  
16          selectively etching the polysilicon layer in the memory  
17          region to define a plurality of polysilicon  
18          structures as word lines having gaps therein, and  
19          removing the polysilicon from the first shallow  
20          trenches and leaving the polysilicon layer in the  
21          second shallow trench in the peripheral circuit  
22          region; and  
23          forming an insulator in the first shallow trenches and  
24          the gaps between the word lines.

1           2.    The method as claimed in claim 1, further  
2 comprising:

3 planarizing the insulator to leave shallow trench  
4 isolations in the first shallow trenches and  
5 between the word lines;  
6 selectively etching the polysilicon structures and the  
7 ONO layer to expose the semiconductor substrate  
8 between the first shallow trenches; and  
9 implanting dopants into the substrate between the first  
10 shallow trenches to define the well regions.

1 3. The method as claimed in claim 1, wherein the bit  
2 lines formation further comprises:

3 forming a first photoresist pattern with a plurality of  
4 parallel first openings on the pad oxide in the  
5 memory region to serve as bit line mask;  
6 implanting dopants into the semiconductor substrate to  
7 form a plurality of parallel buried diffusion  
8 regions as bit lines in the memory region; and  
9 removing the bit line mask.

1 4. The method as claimed in claim 1, wherein the first  
2 and the second shallow trench formation further comprises:

3 forming a second photoresist pattern on the pad oxide,  
4 wherein the second photoresist pattern has second  
5 openings in the peripheral circuit region;  
6 selectively etching the semiconductor substrate through  
7 the second openings to create a first shallow  
8 trench and a second shallow trench; and  
9 removing the second photoresist pattern and the pad  
10 oxide.

1        5.    The method as claimed in claim 1, wherein the  
2 semiconductor substrate is a silicon substrate.

1        6.    The method as claimed in claim 1, wherein the  
2 semiconductor substrate is a silicon-on-insulator (SOI)  
3 substrate.

1        7.    The method as claimed in claim 1, wherein the pad  
2 oxide is formed by thermal oxidation.

1        8.    The method as claimed in claim 1, wherein the  
2 buried diffusion regions are formed by implanting n-type  
3 ions in the semiconductor substrate.

1        9.    The method as claimed in claim 1, wherein the  
2 buried diffusion region is implanted before the ONO layer is  
3 formed.

1        10.   The method as claimed in claim 1, wherein the  
2 buried diffusion region is implanted after the ONO layer is  
3 formed.

1        11.   The method as claimed in claim 1, further  
2 comprising rapid thermal annealing (RTA) after implantation  
3 to activate the dopants in the substrate.

1        12.   The method as claimed in claim 1, wherein the bit  
2 line mask is a patterned photoresist.

1        13.   The method as claimed in claim 1, wherein  
2 thickness of the ONO layer is between about 150 and 250Å.

1           14. The method as claimed in claim 1, wherein the ONO  
2 layer is further formed on the sidewall of the shallow  
3 trench to avoid STI corner recess.

1           15. The method as claimed in claim 1, wherein the ONO  
2 layer is further formed on the sidewall of the shallow  
3 trench to avoid deformation of the STI profile during  
4 thermal process.

1           16. The method as claimed in claim 1, wherein the  
2 insulator is a silicon dioxide layer.

1           17. The apparatus as claimed in claim 16, wherein the  
2 polysilicon layer comprises a dopant polysilicon layer.

1           18. The method as claimed in claim 1, wherein the  
2 insulator is formed by high density plasma chemical vapor  
3 deposition (HDPCVD).

1           19. The method as claimed in claim 2, wherein the  
2 insulator is planarized by chemical mechanical polishing.